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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/472,869	12/28/1999	Tae-Yong Sohn	Q57124	9316

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EXAMINER	
NATNAEL, PAULOS M	

ART UNIT	PAPER NUMBER
2614	17

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/472,869	SOHN, TAE-YONG	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2/10/04.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 and 11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 1-4 is/are allowed.

6)☒ Claim(s) 5 and 11 is/are rejected.

7)☒ Claim(s) 6-9 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **5** and **11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sokawa et al. U.S. Pat. No. 6,353,460.

Considering claim 5, Sokawa et al. disclose the following claimed subject matter, note; a) the claimed video decoder for decoding a video component of a received digital signal into a first input digital signal, is met by digital decoder 1017, fig.1;

b) the claimed analog to digital converter for converting a received analog video signal into a second input digital signal, is implied here because the format conversion section is a digital processing device, not an analog processing device.

c) the claimed a format converter for receiving either of a first input digital signal and a second input digital signal, according to which of the first and second input digital signals is present, the format converter for converting the input digital signal into a

predetermined display format output signal, is met by the format conversion section 1100, fig.1;

d) the claimed controller for detecting a frame rate of the input digital signal received by said format converter and outputting a timing control signal corresponding to the frame rate detected is met by the CPU 1020, fig. 1;

Except for;

e) the clock frequency providing means for providing a clock frequency according to the timing control signal output by said controller, said clock frequency provided to the format converter for converting the input digital signal received by said format converter into said predetermined display output signal, said clock frequency also provided to said video decoder when said second input digital signal is not present at said format converter;

Regarding e), Sokawa et al. disclose that "A clock circuit (not shown) composed of a PLL circuit, for example, for supplying necessary clocks to the respective components of the image processor is also included." (col. 18, lines 32-35) Clock and timing generating devices such as the phase locked loop (PLL) are also well known in the art. Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Sokawa et al. by providing the PLL circuit as suggested by Sokawa and as notoriously well known in the art, in order to properly process and display the received video signal.

Claim **11** is a method claim of claim 5 and, thus, Claim 11 is rejected for the same reasons as in claim 5.

Response to Arguments

3. Applicant's arguments filed 2/10/04 have been fully considered but they are not persuasive. Response follows:

Applicant's arguments

a) Sokawa does not disclose the format converter as claimed... The format conversion section of Sokawa selects one of the video signals as an input, based on the channel selection of a user. By contrast, the format converter of claim 5 receives either the first or the second input digital signal, according to which of the first and second input digital signals is present.

b) Sokawa does not teach or suggest a controller for detecting a frame rate of the input digital signal received by the format converter and outputting a timing control signal corresponding to the frame rate detected.

Examiner's Response

a) The format converter of Sokawa format receives several input signals, signals from V/UHF antenna, a BS antenna, a CS antenna and a PC, as shown in Figure 1. It would be obvious to the skilled in the art that all the signals may not be available all the time. Thus, the system would operate with whatever the input signals might be. Thus, the argument that "the format converter of claim 5 receives either the first or the second

input digital signal, according to which of the first and second input digital signals is present" is incomprehensible and unpersuasive.

b) Sokawa et al discloses that "The processing by the subtracter 2094, the absolute circuit 2096, and the nonlinearization circuit 2098 are performed by the SMID type digital signal processing section (2010, 2012, 2014). More specifically, the DIR 2016 of the SVP receives the input image data from the input section 2040 (FIG. 7) and the image data delayed by one frame from the image memory 2050 (frame memory 2090) simultaneously for each line by synchronizing the one-frame delayed image data with the input image data from the input section 2040. This synchronization can be realized by matching the timing of the reading from the output buffer SDO of the image memory 2050 with the input image data." (col. 26, lines 1-12) Although, Sokawa does not use the term "frame rate" it is evident from above and the disclosure in general that the frame rate of the input signal are taken in consideration and according to such frame rate, the rate at which the frames are written or read from the frame memory 2090 for example, the signals are processed. Therefore, the argument that "Sokawa does not teach or suggest a controller for detecting a frame rate of the input digital signal received by the format converter and outputting a timing control signal corresponding to the frame rate detected" is unpersuasive.

Allowable Subject Matter

4. Claims **1-4** are allowable over the prior art.

5. Claims **6-9** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose a first PLL circuit and a second PLL circuit for generating a first and second clock frequency signals, as in claims 1 and 6;

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
February 13, 2004

MICHAEL H. LEE
PRIMARY EXAMINER